ABSTRACT OF THE DISCLOSURE (CLEAN COPY)

A fast Fourier transform (FFT) operating apparatus and a method thereof carries out an FFT operation in a programmable processor chip. A program controller generates an FFT start signal and controls a programmable processor, and a program memory stores an application of the programmable processor. An FFT address generator removes the looping instruction used for the FFT and a cycle for an address generator, and generates an offset address of a butterfly input data and an operation end signal. An address generator calculates an address of a data memory using the offset address generated in the FFT address generator and a data memory stores data. A data processor carries out an arithmetic and logic operation using the data stored in the data memory and a flag register generates an FFT operation signal.